**SANCHITH PADMARAJ**

Chicago, IL 60616 ∙ (312)8433256∙ spadmaraj@hawk.iit.edu ∙ LinkedIn: www.linkedin.com/in/sanchith-p

**Master of Science Electrical and Electronics Engineering**

*Illinois Institute of Technology, Chicago, IL*  *Expected May 2019* **Concentration: VLSI and Microelectronics** GPA:3.68/4.0

**Bachelor of Engineering Electronics and Communication Engineering** *June 2017*

*SJB Institute of Technology, Bangalore, India* GPA:3.8 /4.0

**SKILLS**

**Programming Language**  C, C++, Assembly language of Microprocessor and Microcontroller

**Operating System:** Windows (98,07,10), LINUX (Ubuntu, RedHat)

**Microsoft Office Package:** Word, Excel, Access, PowerPoint, Publisher

**Software:**  Cadence Virtuoso (ASIC Flow), TCL/TK, Verilog, VHDL, system Verilog Xilinx, MATLAB, NI LabView, P Spice, H Spice, UVM.

**Work experience:**

**Swarm Robotix, Naperville, Illinois May-August 2018**

* Worked as intern.
* Worked in 4G and Xbee communication, between the robots.
* Worked in battery management and building battery for the bots.
* Worked in electrical connection, with the swerve team.
* Skills applied: C,Ros.

**ACADEMIC PROJECTS**

**Verification of Switch RTL core January 2018**

* Developed testcase and interface and integrate with DUT in top module.
* Developed Environment class and include reset and configuration method to reset DUT and configure the port address.
* Developed driver and receiver class to send and receive packets.
* Developed scoreboard for comparison of expected and received packets from DUT.
* Wrote coverage class and testcases.
* Skills applied: System Verilog.

**Design and implementation of a MIPS CPU with multicycle Datapath October 2018**

*Illinois Institute of Technology*

* Designed a custom RISC processor which is basically a stripped-down MIPS processor.
* The processor designed is a 32-bit version of the MIPS processor.
* Implemented the multicycle Datapath version of the processor utilizing the VHDL
* Skills applied: VHDL.

**CAD Tool Design for Time Slack Analysis with Tcl/Tk and C Programming April 2018**

*Illinois Institute of Technology*

* preform slack time analysis using Tcl/tk and C program.
* Used c programming to build the adjacent matrix, find the longest path, and to print the result in text file.
* Used TCL/Tk to read the file, draw the graph and color the vertex of the longest path.
* Skills applied: C, Tcl/Tk.

**FinFET Transistor Characterization and Domino Logic Operation**  **April 2018**

*Illinois Institute of Technology*

* Used hspice to find the delay and the leakage power of inverter in different modes of FinFet.
* Used hspice to find the propagation delay, dynamic power of 4 input AND, OR gate in SG, IG mode of Finfet using domino logic.
* Skills applied: Hspice.

**32-bit Pipelined CPU design November 2017**

*Illinois Institute of Technology*

* Case study of 32-bit CPU design with Different Adders.
* Case study of 32-bit CPU design with Different Adders and 32-bit comparator.
* Skills applied: Verilog, Cadence Virtuoso.

**Diagnosis of Schizophrenia using a Computer Aided January – May 2017**

**Diagnostic tool based on P3b wave characteristics**

*SJB Institute of Technology, Bangalore, India*

* Team consisted of 4 members.
* Designed and developed a Computer Aided Diagnostic tool to objectively discriminate between a healthy. subjects and Schizophrenic subjects.
* Used the obtained data to perform machine learning.
* Skills applied: MATLAB, eeglab, neural networks.

**CERTIFICATION:**

* ‘Emerging Technology: Internet of Things’, organized by The Institute of Engineers, at SJBIT, March 2016.
* ‘Sensorics’ conducted by BOSCH, at SJBIT, January 2016.
* ‘Robotics with Embedded C’, organized by ICUBZ at BMSCE August 2015.
* Soft Skill development training by Zestech, at SJBIT, January-July 2016.